

Task Coarsening Through Polyhedral Compilation for a Macro-Dataflow Programming Model

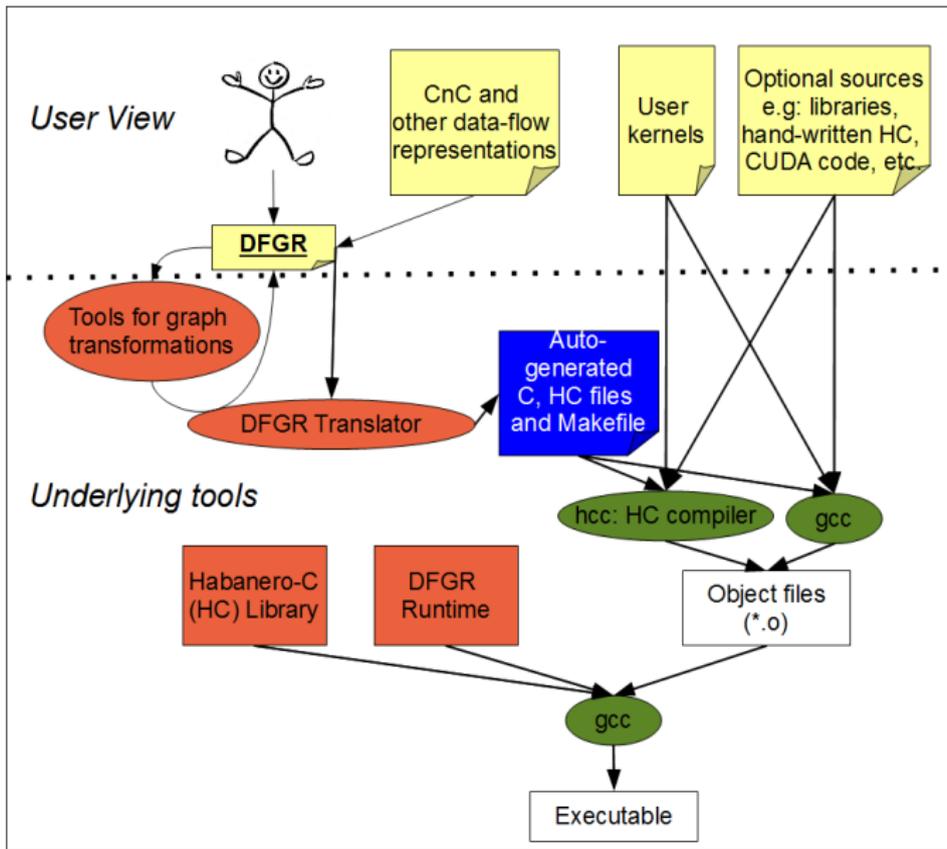
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DFGR and HC



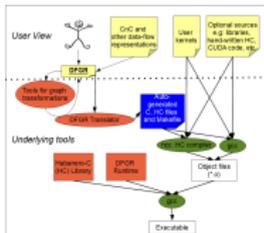
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2015Task Coarsening Through Polyhedral Compilation
for a Macro-Dataflow Programming ModelAlina Sbirlea¹, Louis-Noël Pouchet², Vivek Sarkar¹¹Rice University, ²Ohio State University

DFGR: Data-Flow Graph Representation

DFGR

- Has two components:
 - Textual component:**
 - high-level view for domain experts
 - IR component:**
 - automatic generation from higher-level programming systems
- Uses current software and compilers:
 - Habano-C** provides a parallel task language with extensions for **OpenCL code generation**
 - OCR** for a distributed execution
 - TLDM** generation for FPGAs
- Proposes the use optimizations at the IR level.
- See DFM'14 publication by Sbirlea, Pouchet and Sarkar



DFGR regions as iteration spaces:

a hierarchy of concepts

- Item collection declarations
 - [int* item]; [float* item2];
- Step collection declarations
 - (step1 : a, b) @CPU=val1, GPU=val2, FPGA=val3;
- Step prescriptions
 - (step1 i, j) := (step2 : i+1, j);
- Step I/O relations
 - (step2 : bar(i, j)) -> (step1 : i, j);
 - [item : i, j-1] -> (step1 : i, j+1);
 - (step1 : i, j) -> [item1 : i, j]; [item2 : i+1, j];
- Ranges and Regions
 - [item : {i-1, j+1}, {i-1, j+1}] -> (step1 : i, j);
 - <region : i, j > { i <= i, i <= M, 1 <= j <= N};
 - enc: (step1 : region);
 - <region2(p, q) : i, j > { p-1 <= i <= p+1, q-1 <= j <= q+1};
 - (step1 : i, j) -> [item2 : region2(i, j)];
- Environment
 - env : (step1 : region);
 - env -> [item1 : region]; [item2 : region1] -> env;
- Key Features
 - Steps are functional
 - Item collections implement Dynamic Single Assignment form
 - Data type in collections can be arbitrary (w/ serializers)
 - Dependence between steps with step-to-step dependence or via data dependence
 - Use tags as unique identifiers for step instances and items in collections
 - Tag values may be known only at runtime or at compile-time
 - Natively represent task-level, pipeline and stream parallelism

Transforming DFGR graphs for task+data coarsening

DFGR to Polyhedra

- Support the subset of DFGR programs without non-affine expressions, uninterpreted functions, nor data-dependent guards (e.g. {A, B} <= 0).
- Conversion to polyhedral representation (SCopLib)
 - Create iteration domains by propagating the tag functions in step prescriptions
 - Cache access functions directly from item tag functions
 - No closure needed
- Extract dependence polyhedra: DSA form ensures only flow dependences; no need for any schedule to determine which instance is the producer or consumer for RAW

Polyhedra to Polyhedra

- Transformation objective for DFGR on CPU: increase task granularity to have less tasks computing on more data and reduce communication
- Use iteration space tiling on the polyhedral representation with the PLTo algorithm (Rondodriguez et al. 2005)
- Input is polyhedral representation + dependence polyhedra, run PLTo on it and obtain a schedule for the transformed program as well as tiled iteration domains

Polyhedra to DFGR

- Generate C code implementing the tiled schedule using CLooT [Battos, 2004]
- New DFGR tasks are created for each tile body generated
 - Dependence between tiles are modeled by describing the data flow between tiles (read/writes)
- Data flow of the transformed program extracted by polyhedral analysis, after updating also the data layout with tiling of data in item collections
- DSA on data files may not be generated but the transformed code is still DSA, use "data" item collections to make the DFGR graph DSA if multiple tags write to the same file

Smith-Waterman example

```

C code
A[i][0] = corner(i);
for (j=1; j<NW; j++)
  A[i][j] = top(j);
for (i=1; i<NW; i++) {
  A[i][0] = left(i);
  for (j=1; j<NW; j++)
    A[i][j] = center(i, j, A[i-1][j-1],
      A[i-1][j], A[i][j-1]);
}

```

Dependences



Input DFGR

```

<int* A>
{corner(i, j) -> [A[i], j];
 [A[i-1, j] -> (step1 : j) -> [A[i], j];
 [A[i-1, j-1], [A[i-1, j], [A[i-1, j-1] ->
  [A[i], j];
 env: (corner(i, j) -> [A[i], j];
 env: (step1 : j) -> [NW];
 env: (center(i-1, .. NW), i, 1 .. NW);
 [A[i], NW] -> env;

```

Transformed DFGR

```

<int** A>
{corner2(i, col, col) -> [A, col, col];
 [A, col, col-1] -> (rowstart2 : col, col) -> [A, col, col];
 [A, col-1, col] -> (rowend2 : col-1, col) -> [A, col, col];
 [A, col-1, col-1] -> [A, col-1, col-1];
 env: (rowstart2 : col) -> [NW];
 env: (rowend2 : col) -> [NW];
 env: (center2(i, col, col) -> [max(i, col) - col - floor(NW, 32) +
  rowend2 : col, col] -> [col-2*floor(NW, 32) +
  rowend2 : col, col] -> [col-2*floor(NW, 32) +
  rowend2 : col, col];
 env: (rowstart2 : col, col);
 env: (rowend2 : rowend2, col);
 env: (center2 : rowend2, rowend2);
 env: (rowstart2 : rowend2);

```

Performance results on 16-core Intel E7330 @ 2.4 GHz

